WHAT IS CLAIMED IS:

1. A method comprising:

forming a dielectric layer on a circuitized substrate having a conductive region;

opening the dielectric layer to expose the conductive region;

forming a first solder bump on the conductive region;

forming a diffusion barrier on the first solder bump; and

forming a second solder bump on the first solder bump.

2. The method of Claim 1 wherein the first and second solder bumps each comprise a different solder composition.

3. The method of Claim 1 wherein a reflow temperature of the first solder bump is greater than a reflow temperature of the second solder bump.

4. The method of Claim 1 wherein the dielectric layer is a photoimageable dielectric layer.

5. The method of Claim 1 wherein the circuitized substrate is a semiconductor wafer.

6. The method of Claim 1 wherein said first solder bump includes a generally dome-shaped surface terminating below a top surface of the dielectric layer.

7. The method of Claim 6 wherein said dome-shaped surface partly protrudes above said top surface of the dielectric layer and terminates below the top surface at a defined distance therefrom.

8. The method of Claim 7 wherein said diffusion barrier comprises a thickness having a value generally equal to said defined distance.

9. The method of Claim 8 wherein said diffusion barrier has a top barrier surface and is formed on said dome-shaped surface.

10. The method of Claim 9 wherein said second solder bump covers said diffusion barrier and includes an exterior surface that generally terminates at a juncture point of said top barrier surface of diffusion barrier and said top surface of the dielectric layer.

11. The method of Claim 1 wherein said first solder bump comprises tin and said second solder bump comprises lead and said diffusion barrier comprises a Group VIII B metal.

12. The method of Claims 11 wherein said barrier additionally comprises a coating of a noble metal.

13. An article produced in accordance with the method of Claim 1.

14. An article produced in accordance with the method of Claim 12.

15. An article comprising a substrate; a conductive layer disposed on said substrate; a first solder bump including a generally dome-shaped surface and disposed on said conductive region; a dielectric layer having a top surface and disposed on said substrate; a diffusion barrier disposed on said generally dome-shaped surface; and a second solder bump disposed on said diffusion barrier.

16. The article of Claim 15 wherein said generally dome-shaped surface partly protrudes above said top surface of said dielectric layer terminates below said top surface of said dielectric layer at a defined distance therefrom.

17. The article of Claim 16 wherein said diffusion barrier comprises a thickness having a value generally equal to said defined distance, and said first solder

bump has a higher reflow temperature then a reflow temperature of the second solder bump.

18. The article of Claim 17 wherein said diffusion barrier has a top barrier surface and is formed on said dome-shaped surface, and said second solder bump covers said diffusion barrier and includes an exterior surface that generally terminates at a juncture point of said top barrier surface of diffusion barrier and said top surface of the dielectric layer.

19. The article of Claims 15 wherein said first solder bump comprises tin and said second solder bump comprises lead and said barrier comprises a Group VIII B metal having a noble metal coating.

20. A method comprising:

forming a circuitized substrate having a conductive region;

disposing a first solder bump on the conductive region;

laminating a dielectric layer to the circuitized substrate and on the first solder bump;

abrading the dielectric layer to expose a portion of the first solder bump;

depositing a diffusion barrier on the exposed portion of the first solder bump; and forming a second solder bump on the diffusion barrier.

21. The method of Claim 20 wherein the circuitized substrate is a semiconductor wafer.

22. The method of Claim 20 wherein said abrading additionally comprises abrading the first solder bump to expose the inside of said first solder bump.

23. The method of Claim 22 wherein said inside of said first solder bump comprises an internal planar surface.

24. The method of Claim 23 wherein said internal planar surface is disposed below a top surface of said dielectric layer at a defined distance therefrom.

25. The method of Claim 24 wherein said diffusion barrier is disposed on said internal planar surface.

26. The method of Claim 25 wherein said diffusion barrier comprises a thickness having a value generally equal to said defined distance.

27. The method of Claim 20 wherein said first solder bump comprises tin and said second solder bump comprises lead and said barrier comprises a Group VIII B metal having a noble metal coating.

28. An article produced in accordance with the method of Claim 20.

29. An article comprising a substrate; a conductive layer disposed on said substrate; a first solder bump having an abraded internal planar surface and disposed on said conductive region; a dielectric layer having a top surface and disposed on said substrate; a diffusion barrier disposed on said abraded internal planar surface; and a second solder bump disposed on said diffusion barrier.

30. The article of Claim 29 wherein said abraded internal planar surface is disposed below said top surface of said dielectric layer at a defined distance therefrom.

31. The article of Claim 30 wherein said diffusion barrier comprises a thickness having a value generally equal to said defined distance, and said first solder bump has a higher reflow temperature than a reflow temperature of the second solder bump.

32. The article of Claim 31 wherein said second solder bump covers said diffusion barrier and includes an exterior surface that generally terminates at a juncture point of a top barrier surface of diffusion barrier and said top surface of the dielectric layer.

33. The article of Claim 32 wherein said top barrier surface is generally aligned with said top surface of the dielectric layer.

34. The article of Claim 29 wherein said first solder bump comprises tin and said second solder bump comprises lead and said barrier comprises a Group VIII B metal having a noble metal coating.

35. The method of Claim 7 wherein said defined distance ranges from about 0.01% to about 50% of the value of the thickness of the dielectric layer.

36. The method of Claim 24 wherein said defined distance ranges from about 0.01% to about 50% of the value of the thickness of the dielectric layer.